\*\*\* Running vivado

with args -log full\_adder.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source full\_adder.tcl -notrace

\*\*\*\*\*\* Vivado v2017.3 (64-bit)

\*\*\*\* SW Build 2018833 on Wed Oct 4 19:58:22 MDT 2017

\*\*\*\* IP Build 2016188 on Wed Oct 4 21:52:56 MDT 2017

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source full\_adder.tcl -notrace

Command: open\_checkpoint C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.028 . Memory (MB): peak = 233.289 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 3 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.3

INFO: [Device 21-403] Loading part xc7z020clg484-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/.Xil/Vivado-91968-EL006/dcp3/full\_adder.xdc]

Finished Parsing XDC File [C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/.Xil/Vivado-91968-EL006/dcp3/full\_adder.xdc]

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.069 . Memory (MB): peak = 611.461 ; gain = 0.000

Restored from archive | CPU: 0.000000 secs | Memory: 0.000000 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.069 . Memory (MB): peak = 611.461 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2017.3 (64-bit) build 2018833

open\_checkpoint: Time (s): cpu = 00:00:08 ; elapsed = 00:00:21 . Memory (MB): peak = 611.461 ; gain = 385.598

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.131 . Memory (MB): peak = 613.754 ; gain = 1.914

INFO: [Timing 38-35] Done setting XDC timing constraints.

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.013 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.014 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.015 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.016 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Opt 31-389] Phase BUFG optimization created 0 cells and removed 0 cells

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.016 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1131.324 ; gain = 0.000

Ending Logic Optimization Task | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:01 . Memory (MB): peak = 1131.324 ; gain = 0.000

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 12ee48beb

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.008 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

22 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1131.324 ; gain = 519.863

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.113 . Memory (MB): peak = 1131.324 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file full\_adder\_drc\_opted.rpt -pb full\_adder\_drc\_opted.pb -rpx full\_adder\_drc\_opted.rpx

Command: report\_drc -file full\_adder\_drc\_opted.rpt -pb full\_adder\_drc\_opted.pb -rpx full\_adder\_drc\_opted.rpx

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_drc\_opted.rpt.

report\_drc completed successfully

INFO: [Chipscope 16-241] No debug cores found in the current design.

Before running the implement\_debug\_core command, either use the Set Up Debug wizard (GUI mode)

or use the create\_debug\_core and connect\_debug\_core Tcl commands to insert debug cores into the design.

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 2 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: c5b92cd0

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1131.324 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: c5b92cd0

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.433 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: d8f3155a

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.463 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: d8f3155a

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.465 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 1 Placer Initialization | Checksum: d8f3155a

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.465 . Memory (MB): peak = 1131.324 ; gain = 0.000

Phase 2 Global Placement

Phase 2 Global Placement | Checksum: 19ad5ece6

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.712 . Memory (MB): peak = 1131.953 ; gain = 0.629

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 19ad5ece6

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.714 . Memory (MB): peak = 1131.953 ; gain = 0.629

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 16394c32e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.743 . Memory (MB): peak = 1131.953 ; gain = 0.629

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 19ad5ece6

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.753 . Memory (MB): peak = 1131.953 ; gain = 0.629

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 19ad5ece6

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.753 . Memory (MB): peak = 1131.953 ; gain = 0.629

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 3 Detail Placement | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Phase 4 Post Placement Optimization and Clean-Up | Checksum: d76ba467

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

Ending Placer Task | Checksum: 1cd6b0c8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1135.969 ; gain = 4.645

INFO: [Common 17-83] Releasing license: Implementation

37 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.064 . Memory (MB): peak = 1135.969 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file full\_adder\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.060 . Memory (MB): peak = 1138.652 ; gain = 2.684

INFO: [runtcl-4] Executing : report\_utilization -file full\_adder\_utilization\_placed.rpt -pb full\_adder\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.048 . Memory (MB): peak = 1138.652 ; gain = 0.000

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file full\_adder\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.007 . Memory (MB): peak = 1138.652 ; gain = 0.000

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 2 CPUs

Checksum: PlaceDB: e336a8f ConstDB: 0 ShapeSum: ea34639 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 18e00cc92

Time (s): cpu = 00:00:26 ; elapsed = 00:00:23 . Memory (MB): peak = 1283.578 ; gain = 144.211

Post Restoration Checksum: NetGraph: 99d5a1b5 NumContArr: f42b2add Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 18e00cc92

Time (s): cpu = 00:00:27 ; elapsed = 00:00:23 . Memory (MB): peak = 1290.035 ; gain = 150.668

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 18e00cc92

Time (s): cpu = 00:00:27 ; elapsed = 00:00:23 . Memory (MB): peak = 1290.035 ; gain = 150.668

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: d9c2178c

Time (s): cpu = 00:00:27 ; elapsed = 00:00:23 . Memory (MB): peak = 1293.773 ; gain = 154.406

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 1ed0ac30c

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.773 ; gain = 154.406

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 4 Rip-up And Reroute | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 6 Post Hold Fix | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.00196748 %

Global Horizontal Routing Utilization = 0.00118323 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Utilization threshold used for congestion level computation: 0.85

Congestion Report

North Dir 1x1 Area, Max Cong = 0.900901%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 10.8108%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

Phase 7 Route finalize | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1293.813 ; gain = 154.445

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1295.781 ; gain = 156.414

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 16bda98a8

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1295.781 ; gain = 156.414

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1295.781 ; gain = 156.414

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

49 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:24 . Memory (MB): peak = 1295.781 ; gain = 157.129

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.151 . Memory (MB): peak = 1295.781 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file full\_adder\_drc\_routed.rpt -pb full\_adder\_drc\_routed.pb -rpx full\_adder\_drc\_routed.rpx

Command: report\_drc -file full\_adder\_drc\_routed.rpt -pb full\_adder\_drc\_routed.pb -rpx full\_adder\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file full\_adder\_methodology\_drc\_routed.rpt -pb full\_adder\_methodology\_drc\_routed.pb -rpx full\_adder\_methodology\_drc\_routed.rpx

Command: report\_methodology -file full\_adder\_methodology\_drc\_routed.rpt -pb full\_adder\_methodology\_drc\_routed.pb -rpx full\_adder\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 2 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/full\_adder\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file full\_adder\_power\_routed.rpt -pb full\_adder\_power\_summary\_routed.pb -rpx full\_adder\_power\_routed.rpx

Command: report\_power -file full\_adder\_power\_routed.rpt -pb full\_adder\_power\_summary\_routed.pb -rpx full\_adder\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

60 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file full\_adder\_route\_status.rpt -pb full\_adder\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file full\_adder\_timing\_summary\_routed.rpt -warn\_on\_violation -rpx full\_adder\_timing\_summary\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file full\_adder\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file full\_adder\_clock\_utilization\_routed.rpt

INFO: [Common 17-206] Exiting Vivado at Fri Jan 26 12:33:02 2018...

\*\*\* Running vivado

with args -log full\_adder.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source full\_adder.tcl -notrace

\*\*\*\*\*\* Vivado v2017.3 (64-bit)

\*\*\*\* SW Build 2018833 on Wed Oct 4 19:58:22 MDT 2017

\*\*\*\* IP Build 2016188 on Wed Oct 4 21:52:56 MDT 2017

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source full\_adder.tcl -notrace

Command: open\_checkpoint full\_adder\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.027 . Memory (MB): peak = 232.816 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 3 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.3

INFO: [Device 21-403] Loading part xc7z020clg484-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/.Xil/Vivado-81172-EL006/dcp3/full\_adder.xdc]

Finished Parsing XDC File [C:/Users/eacm3/Desktop/project\_3/project\_3.runs/impl\_1/.Xil/Vivado-81172-EL006/dcp3/full\_adder.xdc]

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.053 . Memory (MB): peak = 612.160 ; gain = 0.000

Restored from archive | CPU: 0.000000 secs | Memory: 0.000000 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.054 . Memory (MB): peak = 612.160 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2017.3 (64-bit) build 2018833

open\_checkpoint: Time (s): cpu = 00:00:08 ; elapsed = 00:00:22 . Memory (MB): peak = 612.164 ; gain = 386.379

Command: write\_bitstream -force full\_adder.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7z020'

Running DRC as a precondition to command write\_bitstream

INFO: [DRC 23-27] Running DRC with 2 threads

WARNING: [DRC ZPS7-1] PS7 block required: The PS7 cell must be used in this Zynq design in order to enable correct default configuration.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Project 1-821] Please set project.enableDesignId to be 'true'.

INFO: [Designutils 20-2272] Running write\_bitstream with 2 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./full\_adder.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

15 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 . Memory (MB): peak = 1078.242 ; gain = 466.078

INFO: [Common 17-206] Exiting Vivado at Fri Jan 26 12:37:04 2018...